TOCOS®
TOCOS-WIRELESS.COM

Data Sheet

Wireless Engine TWE-001STRONG

Version 1.0

External Document

Revision

Version	Date	Notes
1.0	19th Aug 2011	First release

TOCOS®

Contents

1

Product specification

1.1 Overview

TWE-001S-PA

TWE-001S-IP

1.1.1 Product Name

TOCOS Wireless Engine TWE-001STRONG

1.1.2 Part Number

TWE-001S-PA/IP
[PA : Pattern Antenna , IP : IPEX (uFL) Connector]

1.1.3 Introduction

TOCOS Wireless Engine TWE-001 is 2.4GHz RF Module with 10mW output power, which comprises a fast 32bit microcomputer, flash memory, high-performance radio of the IEEE802.15.4 conformity, an embedded antenna (or external antenna through u.FL connector) in a small packaged module.
TWE-001 can be operated with dry cell batteries and has wide variety of peripherals for connectivity of external components such as sensors, a display, LEDs and memory devices.

1.1.4 Main characteristics

- High output power up to 10mW (10dBm).
- Global standard IEEE802.15.4/ZigBee®.
- Long range: (1700m with embedded antenna, 3110m with external 2.0 dbi dipole antenna. *1
- High speed mode: 500/667kbps *2
- Rich memory: RAM 128KB, Flash Memory 512KB.
- Small deep sleeping current: 1.3uA
- Variety of peripherals: 21 (max) Digital I/O, 2 UART, SPI, I2C, 4 ADC, 2 DAC, 2 Comparators.
- 128bit AES accelerator.
- Antenna selection: embedded antenna and external u.FL connector.
- Board to board connector AXT440124 (Panasonic) for power and I/Os.
- Free SDK based on GNU toolchains with Eclipse based IDE provided for original firmware development.
- Runs TWE-Zero applications *3
- RoHS conformance.

**1: the maximum distance may vary depending on its environment.*
**2: the RF physical part is different from IEEE802.15.4 standard, but firmware can be written in the same API. (JenNet, ZigBee PRO is not supported)*
**3: licensed TWE-001 STRONG module is required.*

Use of ZigBee®.

Those who use any intellectual property for business are required to join ZigBee Alliance even TOCOS (a member of ZigBee Alliance) Wireless Engine is used.

Contact ZigBee Alliance for further information.

ZigBee Alliance
http://www.zigbee.org/

FAQ about the membership
http://www.zigbee.org/Join/MembershipFAQ.aspx
（As of August 2010）

4. If my company uses a ZigBee module in my product, do I need to be a member?

Yes.

Note: If firmware is designed without ZigBee (like 802.15.4 API), the manufacture does not need to join the alliance.

1.2 Specification

1.2.1 Chip Set

NXP SEMICONDUCTORS Co., Ltd. JN5148

1.2.2 Antenna

- TWE-001S-PA for board pattern antenna
- TWE-001S-IP for external antenna (u.FL connector)

1.2.3 Radio Standard Specification

- 802.15.4 IEEE conformity (2.4GHz)
- Transmission rate: 250kbps(802.15.4 standard), 500/666kbps
- Channel Number: 15 (11~25)
- Modulation: DS-SS
- Frequency: 2405~2475MHz (center freq.)

1.2.4 Micro Controller

- 32 bits RISC processor
- Variable length op-code for optimal binary size
- Variable CPU clock (4/8/16/32MHz)
- JTAG debugging (supported 802.15.4 MAC API only)
- Watch dog timer
- Brown out detection
- 5 domains of power control
- RAM 128kBytes
- ROM 128kBytes (802.15.4 MAC API, etc)
- Flash memory 512kBytes

1.2.5 Interface

	Number	Description
ADC	4	12bit
DAC	2	12bit
Timer	3	5 modes including PWM output
Pulse counter	2	Running also during sleep mode
UART	2	
SPI bus	1	3 selects master, slave
I2C bus	1	Master, slave
I2S	1	Four wire digital audio
Digital Input / Output	19	Shared with other I/F

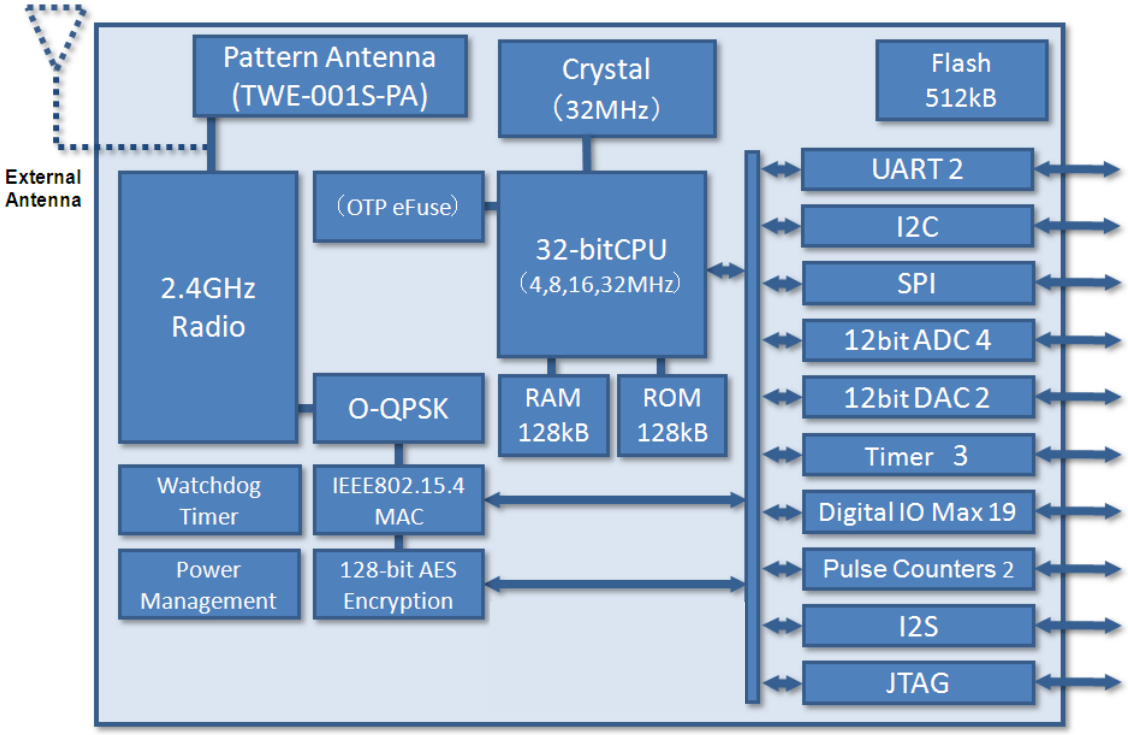
1.2.6 RF Transceiver

	Value	Description
Output Power	+9.08dBm	
Receive sensitivity	-100dBm	25℃,3V,typ
Tx current	28.0mA	25℃,3V,typ, CPU at doze mode
Rx current	23.5mA	25℃,3V,typ, CPU at doze mode
Deep Sleep current	1.36μA	25℃,3V,typ

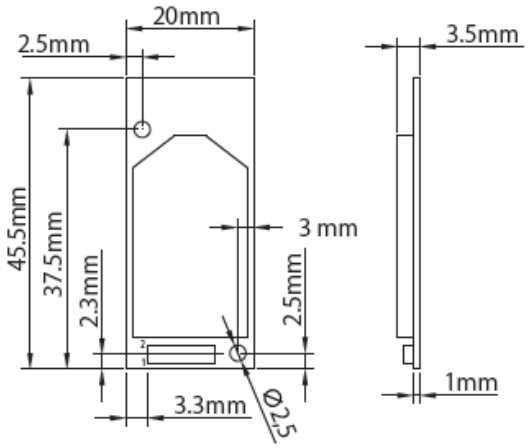
1.2.7 Certification

- RoHS compliance

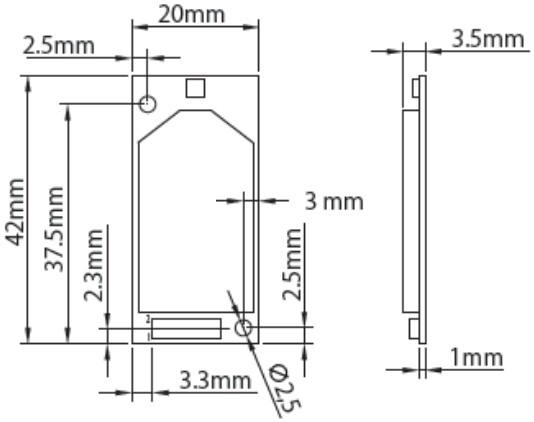
1.3 Block Diagram



1.4 Module Size



TWE-001S-PA
[Pattern Antenna]



TWE-001S-IP
[uFL(IPEX) Connector]

Module Size： 20 x 45.5 x 3.5mm (TWE-001S-PA)
20 x 42 x 3.5mm (TWE-001S-IP)

Weight：4.6g

1.5 Connector

The module side: AXT440124 (0.4mm, 2x20 headers, Panasonic)
Compatible socket: AXT340224

1.6 Pin Configurations

	Signal Name	Signal Type	Description
1	VCC	VCC	Power supply
3	DIO0/SPISEL1	CMOS	DIO0 / SPI Slave Select Output1
5	DIO1/SPISEL2/PC0	CMOS	DIO1 / SPI Slave Select Output 2 / Pulse Counter0 Input
7	SSZ	CMOS	SPI Slave Select Output 0 *1
9	GND	GND	Ground
11	DAC1	Analog	DA converter 1 output
13	C2P	Analog	comparator 2 + input
15	C2M	Analog	comparator 2 - input
17	ADC4	Analog	AD converter 4 input
19	ADC3	Analog	AD converter 3 input
21	DIO7/RXD0/JTAG_TDI	CMOS	Digital IO 7 / UART 0 RX / JTAG Data Input
23	DIO8/TIM0CK_GT/PC1	CMOS	Digital IO 8 / Timer 0 clock gate input / pulse counter 1 input
25	ADC2	Analog	AD converter 2 input
27	ADC1	Analog	AD converter 1 input
29	DIO10/TIM0OUT	CMOS	Digital IO 10 / Timer 0 PWM Output
31	DIO9/TIM0CAP	CMOS	Digital IO 9 / Timer 0 capture input
33	DIO16/IP_DI	CMOS	Digital IO 16 / SPI Slave input
35	DIOO17/CTS1/IP_SEL DAI_SCK/JTAG_TCK	CMOS	Digital IO 17 / UART 1 Clear To Send Input / Intelligent Peripheral Device Select Input / Digital Audio Clock / JTAG CLK
37	DIO18/RTS1/IP_INT DAI_SDOUT/JTAG_TMS	CMOS	Digital IO 18 / UART 1 Request To Send Output / Peripheral Interrupt Output / Digital Audio Data Output / JTAG Mode Select
39	DIO19/TXD1/JTAG_TDO	CMOS	Digital IO 19 / UART 1 Transmit Data Output / JTAG Data Out

	Signal Name	Signal Type	Description
2	DIO2/SPISEL3	CMOS	N/A
4	DAC2	Analog	DA Converter 2 output
6	DIO20/RXD1/JTAG_TDI	CMOS	Digital IO 20 / UART1 RX / JTAG data input
8	DIO3/SPISEL4	CMOS	N/A
10	SWP	CMOS	Built-in flash memory WP When set SWP pin as Low, this affect write protection behavior in M25P40. See the M25P40 datasheet for details.
12	SPIMISO	CMOS	SPI Master Input Slave Out
14	RESETN	CMOS	Reset input (Lo: RESET, Hi:Active)
16	SSM	CMOS	Built-in flash memory SPI Select *1
18	DIO4/CTS0/JTAG_TCK	CMOS	Digital IO 4 / UART 0 CTS / JTAG CLK
20	DIO5/RTS0/JTAG_TMS	CMOS	Digital IO 5 / UART 0 RTS / JTAG Mode Select
22	DIO6/TXD0/JTAG_TDO	CMOS	Digital IO 6 / UART 0 TX / JTAG Data Output
24	DIO15/SIF_D/IP_DO	CMOS	Digital IO15 / Serial Interface Data / Intelligent Peripheral Data Out
26	SPICLK	CMOS	SPI Master Clock
28	DIO14/SIF_CLK/IP_CLK	CMOS	DIO14, Serial Interface Clock / Intelligent Peripheral Clock Input
30	SPIMOSI	CMOS	SPI Master Out Slave In
32	DIO11/TIM1CK_GT/TIM2OUT	CMOS	Digital IO11 / Timer1 Clock Gate Input / Timer2 PWM Output
34	DIO12/TIM1CAP DAI_WS	CMOS	Digital IO12 / Timer1 Capture Input / Digital Audio Word Select
36	DIO13/TIM1OUT DAI_SDIN	CMOS	Digital IO13 / Timer1 PWM Output / Digital Audio Data Input
38	C1P	Analog	Comparator 1 + inputs
40	C1M	Analog	Comparator 1 - inputs

*1 *SSZ and SSM should be wired in order to activate internal flash boot.*

1.7 Maximum Ratings

Parameter	min	Max	
Device supply voltage (VCC)	-0.3	3.6	V
Analog IO(ADC/DAC/COMP)	-0.3	VCC+0.3	V
Digital IO DIO0-8/DIO11-20/RESETN SPICLK/SPIMISO/SPIMOSI/SSZ	-0.3	Lower of (VCC + 2) and 5.5	V
DIO9-10	-0.3	VCC+0.3	V
WP/SSM	-0.3	VCC+0.3	V
Storage temperature	-40	85	℃

1.8 Electrical Characteristics

Parameter	Symbol	Conditions	min	typ	max	
Device supply voltage (VCC)	VCC	Flash device require > 2.3 V	2.0	2.7	3.6	V
Cold Boot voltage		Require flash access	2.3			V
Operating Temperature	T_{OPR}	No dew condensation	-40	25	85	℃
Current	I_{CC}	Deep Sleep		1.36		μA
		Tx (CPU doze),25℃,3V		32.2		mA
		Tx(CPU ACTIVE),25℃,3V		28.0		
		Rx (CPU doze) ,25℃,3V		23.5		
		Rx(CPU ACTIVE) ,25℃,3V		27.7		
DIO Internal pull up		25℃,3V	24	40	63	kΩ
DIO Hi Input	V_{IH}		VCCx0.7			V
DIO Lo Input	V_{IL}				VCCx0.27	
DIO Input Hysteresis			140	230	310	mV
DIO Hi Output	V_{OH}		VCCx0.8			V
DIO Lo Output	V_{OL}				0.4	
Internal DIO pull up Resistors	I_{OL}	VCC 2.7~3.6V		4		mA
		VCC 2.2~2.7V		3		
		VCC 2.0~2.2V		2.5		
Reference Voltage	V_{REF}			1.19		V
ADC Resolution				12		Bits
ADC Integral nonlinearity				±5		LSB
ADC Differential nonlinearity			-1		+2	LSB
ADC Offset error				+10		mV
ADC Gain error				-20		mV
ADC clock				500		kHz
ADC Input voltage range			0.04		V_{REF} $2xV_{REF}$	V

1.9 Various Specifications

Parameter	Specifications
SPI (3 selects , master or slave)	Max 16MHz
Timer	16MHz, 16bit Resolution
Pulse Counters	Max 100kHz, 16bit
UART interfaces	16550A compatible
JTAG Debug Interface	IEEE1149.1 Conformity
Two-Wire Serial Interface (I^2C,SMBUS compatible, master or slave)	Max 100kHz or 400kHz 7/10bit address mode
Four-Wire Digital Audio (I^2S compatible)	Max 8MHz, 16bit, 2ch
Random Number Generator	16bit
Security processor	AES 128bit
Sample FIFO	Accessible to I^2S
Power supply management	Digital / Analog / RAM / Radio / CPU

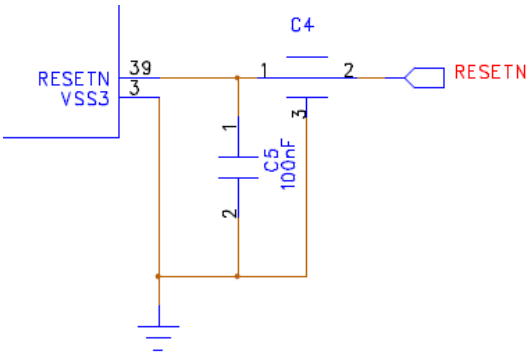
1.10 Antenna

Manufacturer	Antenna	Model Name	Connector
Wieson	Dipole	GY111	IPEX
TOCOS	Reverse-F	PCB Antenna	N/A

Note: Ask sales/distributor to get complete information of available antenna under radio certification.

1.11 Internal Circuit

The RESETN line has EMI filter as below.



* C4 EMI Filter (MURATA NFM18CC223R1C3D)

1.12 Compatibility with the TWE-001

TWE-001 (regular) and TWE-001 STRONG has compatibility except items as below:

- TWE-001 STRONG does not have DIO2/DIO3.
- TWE-001 STRONG is larger than TWE-001 (regular)

TWE-001 (regular)	20 x **40** x 3.5mm(TWE-001-PA/IP)
TWE-001 STRONG	20 x **45.5** x 3.5mm(TWE-001S-PA)
	20 x **42** x 3.5mm(TWE-001S-IP)

- The amplifier activation API needs to be called for TWE-001 STRONG.

1.13 PCB Antenna Guidelines

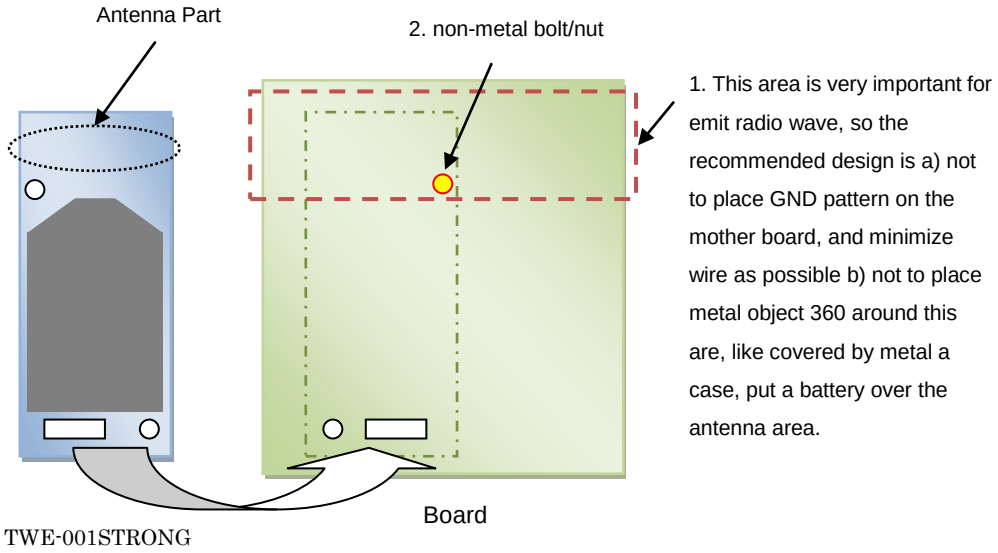
The following guideline should be followed to maximize the performance of PCB antenna.

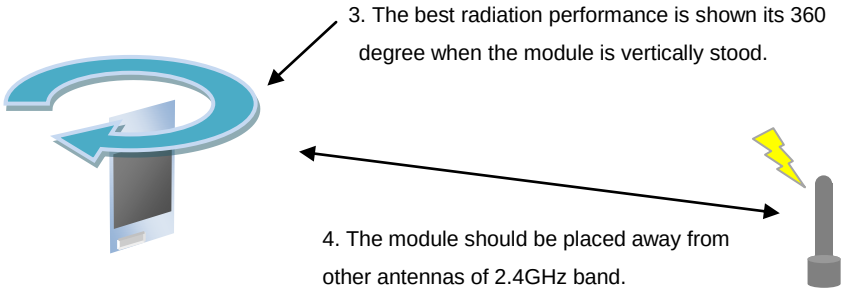
1. The metal object should not be placed around PCB antenna pattern. The un-recommended items are, for example, surrounded by metal case; place a big battery near the antenna or putting a big ground plane below the antenna.

2. Plastic bolt/nut should be used for a screw hole at antenna side to mount a module firmly.

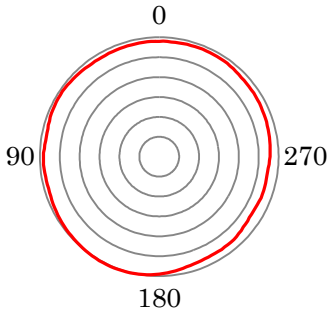
3. The radiation pattern should be considered. Generally the performance is maximized if the antenna is vertically stood.

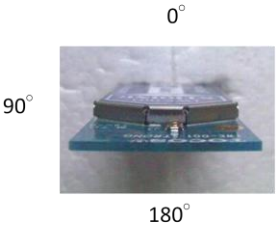
4. The antenna should be kept apart from other antennas of same frequency band.

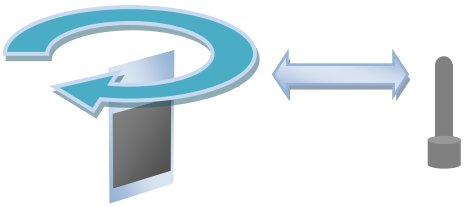


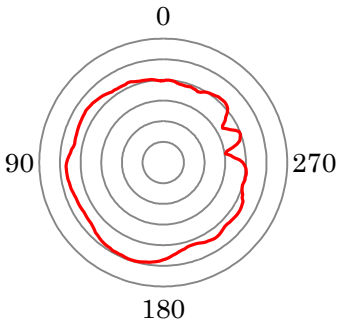


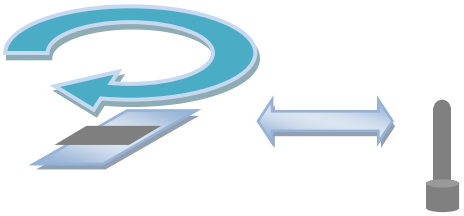
1.14 Radiation Pattern of PCB antenna

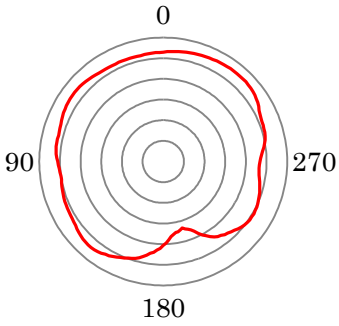


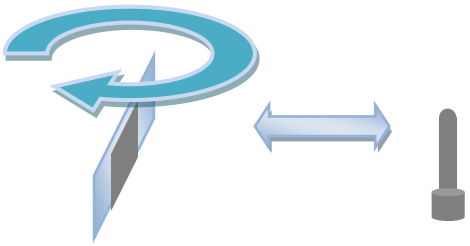








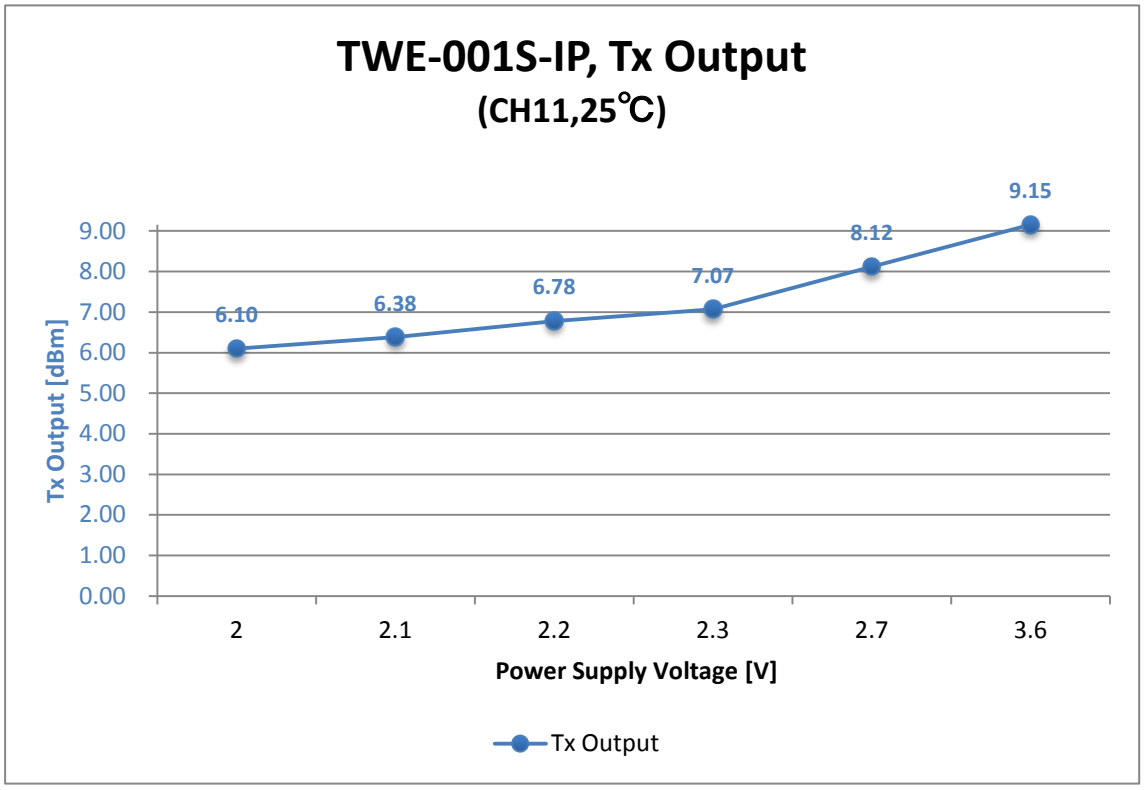




Note: One tick circle represents 10db difference.

1.15 RF Output Power Characteristics

The output power of The TWE-001 STRONG is optimized at around 3.0V or above. The power decreases when the supply voltage gets lower.



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